

Physics 323

Experiment # 8 - Small Signal Amplifier

Purpose

You will design a small signal amplifier to match a set of specifications. You will use the same transistor that you used in the previous two labs.

Prelab

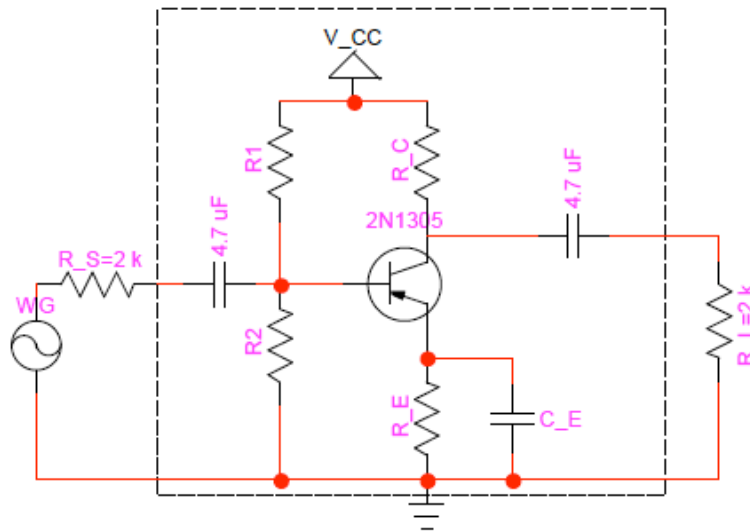


Figure 1: The model circuit for your small signal amplifier

Here are the specifications for your amplifier (in roughly the order you will need to consider them for the design).

1. DC potential available at $V_{CC} = -12$ V
2. For stability $-V_E = 1$ V (a quiescent value)
3. Base voltage range $-V_B = 1.15$ - 1.20 V
4. Current through R_1 : R_2 network greater than $10 \times I_B$
5. Load resistance 2 k Ω
6. Source characteristics: $R_S = 2$ k Ω with an output of $v_s = 10$ mV into the 2 k Ω resistor.
7. v_l/v_s (source to load voltage gain) > 22 dB
8. Low frequency cut-off 90 Hz

Note: I am trying to stick with the convention of negatively-labeled variables for DC (capitalized) voltages and currents for the pnp transistor. This means you will have formulas that have lots of negative signs but when you put in the numbers those extra signs should disappear.

Here is what you need to do:

1. Pick a $-V_C$ to give you the maximum available “swing voltage” knowing that you want to keep $-V_{CE}$ large enough to stay out of the saturation region on the output characteristics (look at your plot from Experiment #6) and you want to keep $-V_E=1$ V. (See page 424 and pages 407-410.) I also included a 1 V margin for $-V_{CC}$.

This results in the following formula

$$-V_C = \frac{(-V_{CC} - 1) + (-V_{E,\min} + (-V_{CE,\min}))}{2}$$

With the assumption that all of the voltage variables are labeled with a negative sign. So the numbers that you put in for the negatively labeled variable should be *positive* e.g.

$$-V_C = \frac{(-V_{CC} - 1) + (-V_{E,\min} + (-V_{CE,\min}))}{2} = \frac{(12 - 1) + (1 + 0.5)}{2} = \frac{11 + 1.5}{2} = 6.25$$

2. Pick $-I_C$ so you have a good operating point (again pages 407-410 will help guide you and if you are really stuck just go with experience). If you want to draw a load line the $y=mx+b$ form is

$$-I_C = \frac{-1}{R_E + R_C}(-V_{CE}) + \frac{-V_{CC}}{R_E + R_C}$$

The load line will intersecting the operating point that you choose and the point $-V_{CE} = -V_{CC}$ on the x -axis of the output characteristic ($-I_C=0$). Using a ruler to rotate around the point $(-V_{CC}, 0)$ is useful.

3. Now you know $-V_{CE}$, $-I_C$, and $-V_{CC}$ you can determine R_E+R_C .
4. Since you know $-V_E$ and $-I_C$ you can determine R_E (and R_C).
5. Since you know $-I_C$ and h_{FE} you can determine $-I_B$. (Find h_{FE} from your measurements in Lab #6; it probably best to use a value for h_{FE} that is at your operating point i.e. $\frac{-I_C}{-I_B}$ rather than the multimeter value.)
6. Now find the lower limit for $R_1 + R_2$ given the limit on the minimum current through this network (Specification #4 above) e.g. suppose that $-I_B=14 \mu\text{A}$, you want at least 140 μA to pass through the R_1 and R_2 voltage divider. The voltage across the divider is $-V_{CC}$ so the *maximum* permissible sum for $R_1 + R_2$ is

$$(R_1 + R_2)_{\max} = \frac{-V_{CC}}{10(-I_B)} = \frac{12 \text{ V}}{0.14 \text{ mA}} = 86 \text{ k}\Omega$$

7. Find the desired value of $-V_{BE}$ from the input characteristic and hence the desired $-V_B$.
8. Find the ratio of R_1 and R_2 to give the correct base voltage.

$$\frac{R_1}{R_2} = \frac{-V_{CC}}{-V_B} - 1$$

(don't let R_2 get too small or your input resistance will get to small!)

9. Now determine appropriate values for R_1 and R_2 . Calling the results of the two previous formulas *sum* and *ratio* we find the optimum values

$$R_{1,\max} = \text{sum} \left(\frac{\text{ratio}}{1 + \text{ratio}} \right)$$

$$R_{2,\max} = \frac{R_{1,\max}}{\text{ratio}} = \frac{\text{sum}}{1 + \text{ratio}}$$

These are *guides*; once you have these calculations just try and choose resistor values that are close. Err on the side of making R_1 slightly smaller (10 to 15% isn't a problem) and then choose R_2 to get the correct *ratio*.

10. There isn't a specified upper limit for the voltage gain and there are going to be significant loading effects (*Why? You should have a very precise answer to this question!*) To maximize the gain we will use the *decoupling* capacitor C_E which will determine the low frequency cutoff (note: not the same cutoff that comes from the *coupling* capacitor that I had you measure last week). Determine $g_m = h_{FE}/h_{ie}$ from Experiment #6. Now $r_e = 1/g_m$. The lower frequency cutoff is given in the specifications. Use formula 18.23 to determine the lower limit for C_E .
11. I have chosen values for the coupling capacitors that suit your needs. They shouldn't effect any of the measurements in the 20 Hz- 500 kHz frequency range.
12. Once this is complete predict the voltage gain that comes from the ratio of voltage applied to the load to the voltage from the source (i.e loading effects at the input and output are included). This calculation involves effective input and output small signal resistances which I have labeled with single primes (')

$$R'_i = R_1 // R_2 // h_{ie}$$

$$R'_o = R_C // (h_{oe})^{-1}$$

$$\frac{v_l}{v_s} = -g_m R'_o \left(\frac{R'_i}{R_S + R'_i} \right) \left(\frac{R_L}{R_L + R'_o} \right)$$

The fractions in the final expression are voltage divider terms. (yes, you need to find h_{oe} from the slope of the output curves in Exp. 6.)

13. Also predict the current gain i_l/i_s . You will be using different effective resistances that I have labeled with *double primes*

$$R_i'' = R_1 // R_2$$

$$R_o'' = R_C // (h_{oe})^{-1}$$

$$\frac{i_l}{i_s} = -h_{FE} \left(\frac{R_i''}{R_i'' + h_{ie}} \right) \left(\frac{R_o''}{R_o'' + R_L} \right)$$

The fractions in the final expression are now current divider terms. In my experience this prediction for current gain will be closer to the measured value than the voltage gain prediction since uncertainties in h_{ie} play a smaller role.

14. The small signal input impedance is given by the expression for R_i' and the small signal output impedance is given by the expression for R_o'' or R_i' (same expression). Calculate both of them if you haven't already.

Lab

Construct the bias circuit for the amplifier. Measure and compare the Q-point values to your prediction. Use a Simpson meter for the measurement of base current but remove it when you are finished. Make sure everything makes sense before making the AC measurements!

Now connect the wave generator with R_S to the input and R_L to the output. In order to get $v_s = 10$ mV peak-to-peak you will need to turn the wave generator amplitude to its minimum setting and use both -20 dB controls. Set the frequency to 2 kHz. Measure the voltage gain $A_v = (v_l/v_s)$, the current gain $A_i = i_l/i_s$, the effective input resistance, and the effective output resistance. Also by measuring V_E verify that the AC component is shorted out by the decoupling capacitor. If you get confused try simplifying the circuit until you understand what you are measuring.

Measure gain and phase responses for your amplifier for the frequency range 20 Hz - 500 kHz. You do not need to make a lot of measurements "mid-band" where the gain doesn't change but take more measurements near the low and high frequency cutoffs so that you can estimate the cutoff frequencies from your graphs. You should be able to see the upper frequency cutoff that comes from the stray capacitance in the transistor. Make an estimate of that capacitance. Make a plot of dB gain vs $\log f$ and phase vs $\log f$. Since the basic amplifier is inverting you will expect the phase to be 180° in the mid-band. What is the bandwidth of the amplifier?