Final Exam: Electronics 323
April 19, 2010

Formula sheet provided. In all questions give at least some explanation of what you are doing to receive full value. You may answer some questions ON the question sheet so please return all materials. Total 84 points. Individual values follow each question.

1. (a) Consider an n-channel enhancement MOSFET as shown in Fig. 1. Please label the components and their compositions on the figure and explain how the MOSFET works. (6)

   (b) CMOS logic depends using pairs of n-channel and p-channel enhancement MOSFETs. The convention is that an n-channel enhancement MOSFET is designated by an arrow pointed inward and the MOSFET is "ON" when $V_{GS} > 0$. (Opposite convention for a p-channel enhancement MOSFET.) With this in mind give the logical truth table for the circuit in Fig. 2 for inputs A and B and output X with 0 representing low voltage and 1 representing a finite positive voltage. Explain your reasoning. Again if you want to answer directly below the figure to save re-drawing the circuit feel free. What kind of logic gate is this? (8)

2. Consider the circuit in Fig. 3.

   (a) What is the difference between combinatorial and sequential logic? (2)

   (b) Explain what happens for different input conditions for the circuit in Fig. 3. What kind of circuit is this? (Just the name; I don't need specific stuff like "active high" or "edge triggered".) (5)

   (c) What is the "toggle" function when referring to a flip-flop? What kind of flip-flop has this function? (3)

3. A *junction gate field effect transistor* or JFET can be used as a constant current source (or drain) or as a voltage-controlled variable resistor. An n-channel JFET is operated by setting $V_{GS} \leq 0$ (i.e. reverse biasing the p-type gate relative to the n-type substrate) which restricts the flow of current.

   (a) Provide some sketches of the output characteristics of the n-channel JFET (I_D versus V_{DS} for different values of V_{GS}). I am not so concerned about a quantitative sketch here but if you like you may consider that I_{DSS}=8 mA and $V_P = -5$ V. (3)

   (b) Now consider the circuit in Fig. 4 which is meant to act as a constant-current drain for the load, R_L. Determine I_D using the values above and on the figure if $R_L = 2$ kΩ. (Quadratic equation alert! You will want the solution for V_{GS} that is negative but is higher than V_P.) If you have trouble with the equation draw a graph to show how you find a solution for I_D. Why would this be called a constant current drain? (7)

4. Why is an intrinsic semiconductor different from a normal metallic conductor? How do you make a semiconductor "p-type" and "n-type"? Suppose that p and n type semiconductors are in contact with each other. Make a sketch of the total carrier concentration across the junction. What is the central region called? (8)

5. Consider the transistor amplifier circuit shown in Fig. 5. The h_{fe} of the transistor is 80. $h_{oe} = 80$ μS. It is a silicon-based transistor.

(a) Stating your assumptions calculate the DC or quiescent current through the collector resistor and also calculate V_o. (4)

(b) I assume one of the assumptions you used was that I_B was small compared to the current through the voltage divider. Verify this assumption. (2)

(c) Construct the small signal h-parameter model neglecting h_{re} and calculate the small signal voltage gain (should agree with equation 32 on the formula sheet). Again state your assumptions. (6)

(d) This ciruit uses negative feedback and one benefit of negative feedback is to increase input resistance. By employing the small signal model verify that equations 34 and 35 on the formula sheet are correct. (Hints: you need to find a relationship between v_b and i_b so you are "looking into" the base. Use the $h_{fe}i_b$ expression for the constant current generator and assume that R_E carries this current plus the base current.) (6)

(e) Where would you include a "coupling capacitor"? What is its purpose? Give a value for C such that the lower frequency cutoff (a 3 dB point) for the input is 80 Hz assuming a small source resistance. (4)

(f) Where would you include a "decoupling" capacitor? What would be the benefit? (2)

6. (a) Name a use for a diode in a ciruit and give an example circuit. (4)

(b) Very briefly, how does a BJT work i.e. explain transistor action or why there is such a quantity as h_{FE}. (4)

(c) Consider the op-amp ciruit in Fig. 6. Derive an expression for the gain and state your assumptions. (6)

(d) What is a "3 dB" point? Make a sketch to illustrate how you would find it from a graph. (4)

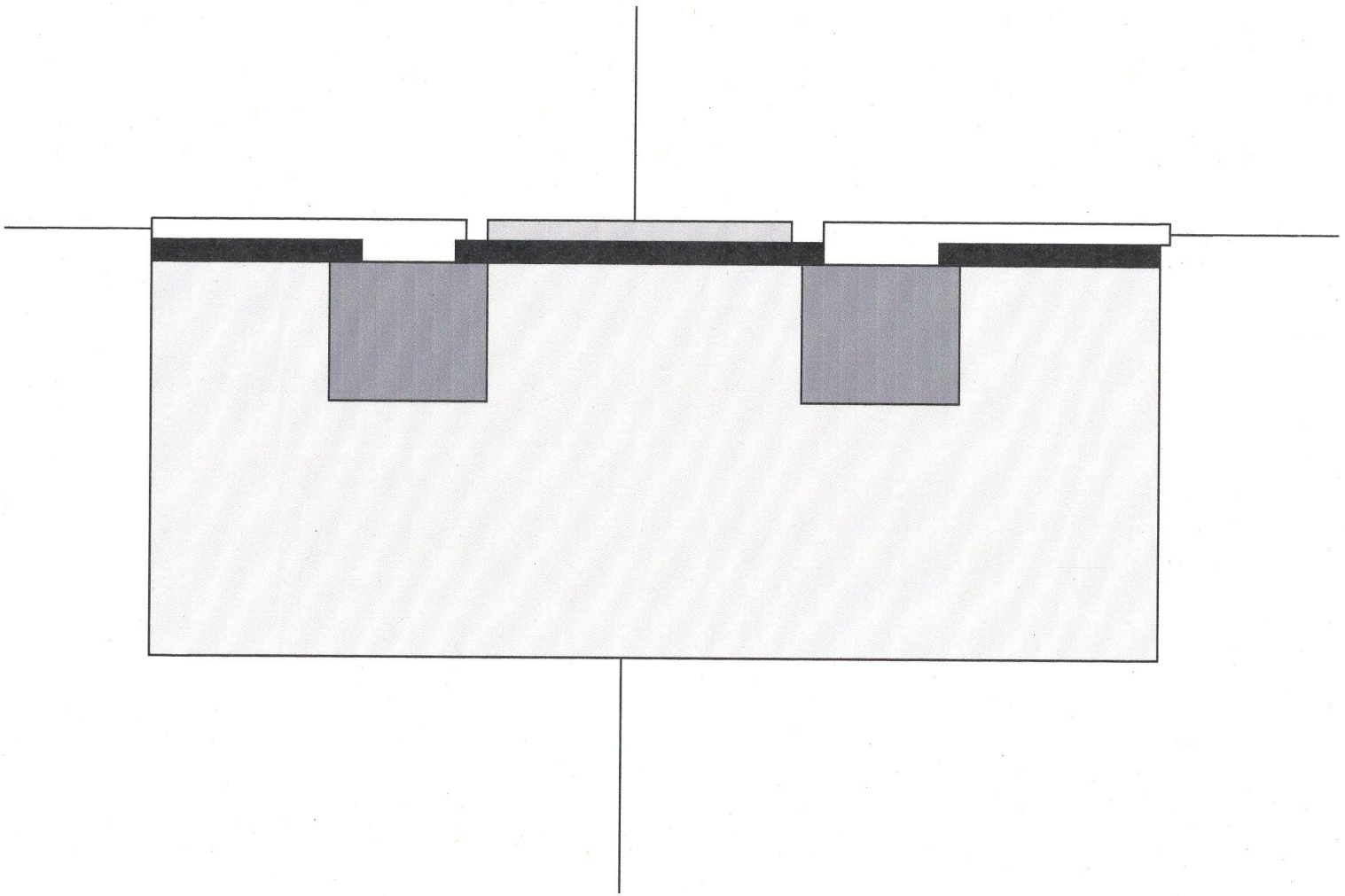

Fig. 1: n–channel enhancement MOSFET (you provide the labels!)

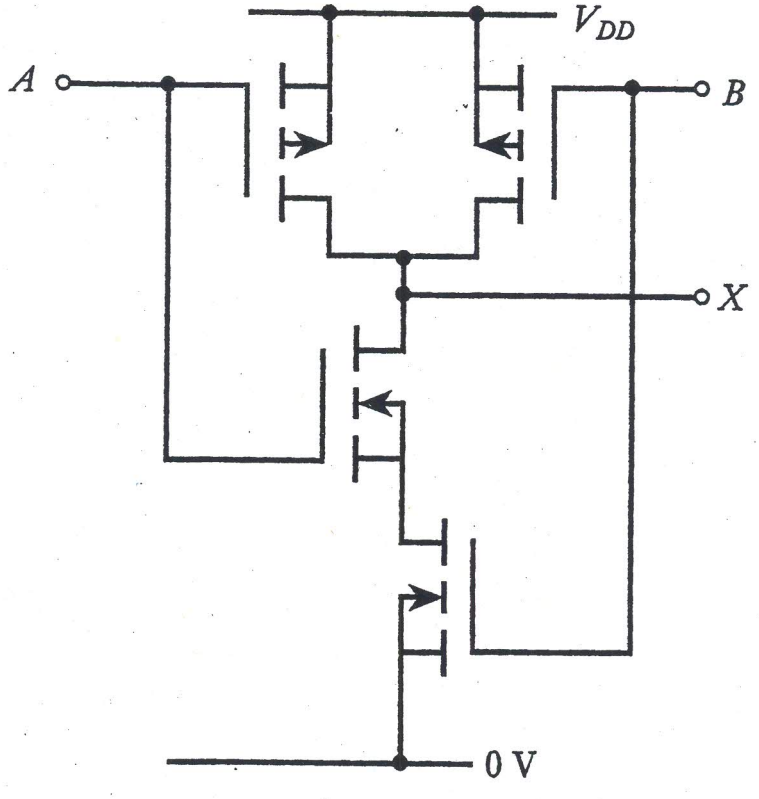

Fig 2: A CMOS logic gate

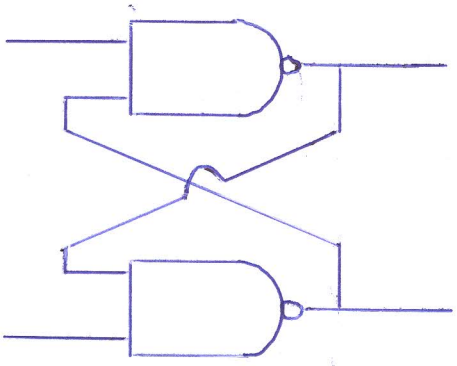

Fig 3: Circuit with two inputs and two outputs.

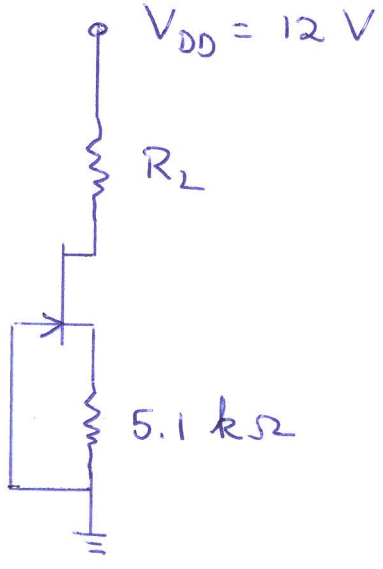

Fig 4: Constant current drain with an n-channel JFET.

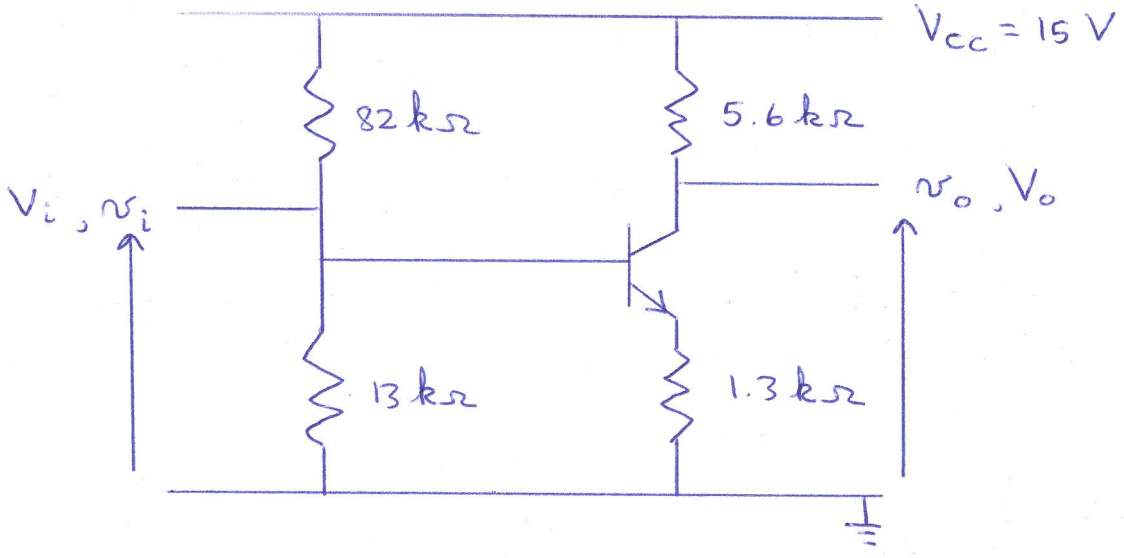

Fig. 5 : Transistor Amplifier Circuit

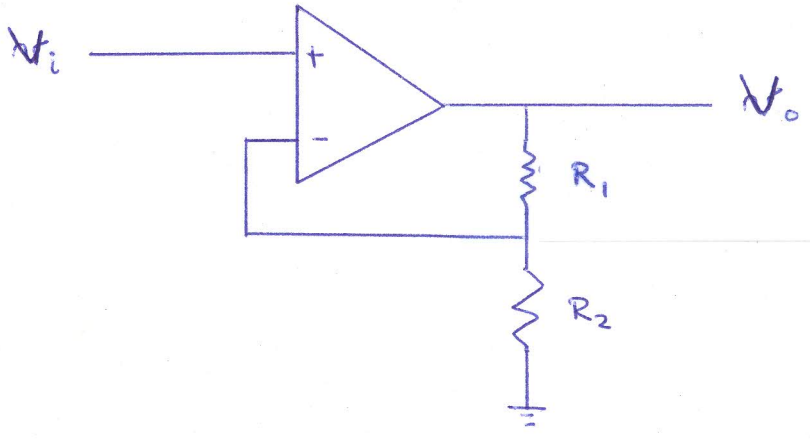

Fig. 6 : Op-Amp Circuit

$$V_{\text{amplitude}} = \sqrt{2}\, V_{RMS} \tag{1}$$

$$A_V = \frac{V_{out}}{V_{in}} \tag{2}$$

$$A_V(\text{ideal}) = \frac{V_{out,\text{OC}}}{V_{in}} \tag{3}$$

$$V = IR \tag{4}$$

$$R_{Th} = R_N = \frac{V_{\text{OC}}}{I_{\text{SC}}} \tag{5}$$

$$\text{Gain (dB)} = 10 \log_{10} \frac{P_2}{P_1} \stackrel{*}{=} 20 \log_{10} \frac{V_2}{V_1} \tag{6}$$

$$\begin{aligned} Z_R &= R & (7)\\ Z_C &= (j\omega C)^{-1} & (8)\\ Z_L &= j\omega L & (9) \end{aligned}$$

$$\text{Gain (closed-loop)} = \frac{A}{1 + AB} \tag{10}$$

$$f_{3\text{dB}} = (2\pi RC)^{-1} = (2\pi\tau)^{-1} \tag{11}$$

$$\text{Gain (non-inverting)} = \frac{R_1 + R_2}{R_2} \ \text{, (R_1 connected to the output)} \tag{12}$$

$$\text{Gain (inverting)} = -\frac{R_1}{R_2} \ \text{, (R_1 connected to the output)} \tag{13}$$

$$V_{out}(t) = -\frac{1}{RC} \int_0^t dt'\, V_{in}(t') + \text{constant} \tag{14}$$

$$V_{out} = -RC\, \frac{dV_{in}(t)}{dt} \tag{15}$$

$$V_{out} = -(V_1 + V_2)\frac{R_1}{R_2} \ \text{, (R_1 connected to the output)} \tag{16}$$

$$V_{out} = (V_1 - V_2)\frac{R_1}{R_2} \ \text{, (R_1 connected to output and ground)} \tag{17}$$

$$\text{(Gain)(Bandwidth)} \sim \text{(unity gain bandwidth)} \tag{18}$$

$$\frac{S}{N}\text{ratio} = 20 \log_{10} \left(\frac{V_S}{V_N} \right) \tag{19}$$

$$\vec{J} = \sigma \vec{E} \tag{20}$$

$$\sigma = e(n\mu_e + p\mu_h) \tag{21}$$

$$np = 4 \left(\frac{k_B T}{2\pi\hbar^2} \right)^3 (m_e m_h)^{3/2} \exp\left(-\frac{E_g}{k_B T} \right) \tag{22}$$

$$n_i = p_i \tag{23}$$

$$I = C \exp\left(-\frac{e(V_0 - V)}{k_B T} \right) - I_S = I_S \left\{ \exp\left(-\frac{e(V_0 - V)}{k_B T} \right) - 1 \right\} \approx I_S \exp(40\, V) \tag{24}$$

$$I_C = h_{FE} I_B \tag{25}$$

$$I_C \approx I_E \tag{26}$$

$$h_{fe} \approx h_{FE} \tag{27}$$

$$g_m = \frac{dI_C}{dV_{BE}} \approx 40 I_C = \frac{1}{r_e} \tag{28}$$

$$h_{ie} \approx \frac{1}{40 I_B} = \frac{h_{fe}}{g_m} \tag{29}$$

$$dI_C = \left(\frac{\partial I_C}{\partial I_B}\right)_{V_{CE}} dI_B + \left(\frac{\partial I_C}{\partial V_{CE}}\right)_{I_B} dV_{CE} = h_{fe}\, dI_B + h_{oe}\, dV_{CE} \tag{30}$$

$$dV_{BE} = \left(\frac{\partial V_{BE}}{\partial I_B}\right)_{V_{CE}} dI_B + \left(\frac{\partial V_{BE}}{\partial V_{CE}}\right)_{I_B} dV_{CE} = h_{ie}\, dI_B + h_{re}\, dV_{CE} \tag{31}$$

$$A_V \approx -\frac{R_C}{R_E + r_e} \text{ (feedback config)} \tag{32}$$

$$A_V \approx -\frac{R_C}{r_e} \text{ (common emitter or decoup. cap.)} \tag{33}$$

$$r_i = R_1 // R_2 // r_b \tag{34}$$

$$r_b = h_{ie} + (h_{fe} + 1) R_E \text{ (common emitter)} \tag{35}$$

$$r_o = R_C \left(\frac{1 + h_{oe} R_E}{1 + h_{oe}(R_E + R_C)}\right) \tag{36}$$

$$f_c = \{2\pi C_{in}(R_{\text{source}} + r_i)\}^{-1} \text{ (coupling capacitor)} \tag{37}$$

$$f_{co} = \{2\pi C_E (R_E // r_e)\}^{-1} \text{ (decoupling capacitor)} \tag{38}$$

$$f_\beta = \{2\pi (C_{b'e} + C_{b'c}) r_{b'e}\}^{-1} \text{ (high-f hybrid-}\pi\text{)} \tag{39}$$

$$f_\beta \approx \frac{40 I_E}{2\pi h_{fe(0)} C_{b'e}} \tag{40}$$

$$f_T \approx \frac{40 I_E}{2\pi C_{b'e}} \tag{41}$$

$$\frac{V_o}{V_i} = \left\{1 - \frac{5}{(\omega CR)^2} - j\left(\frac{6}{\omega CR} - \frac{1}{(\omega CR)^3}\right)\right\}^{-1} \tag{42}$$

$$f = \frac{1}{2\pi CR\sqrt{6}} \text{ (phase-shift oscillator)} \tag{43}$$

$$A_V = -\frac{1}{29} \text{ (feedback } B \text{ of phase-shift oscillator)} \tag{44}$$

$$\frac{V_o}{V_i} = \left\{3 - j\left(\frac{1 - \omega^2 R^2 C^2}{\omega CR}\right)\right\}^{-1} \text{ (Wein-bridge oscillator)} \tag{45}$$

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 \tag{46}$$