Final Exam: Electronics 323
December 14, 2010

Formula sheet provided. In all questions give at least some explanation of what you are doing to receive full value. You may answer some questions ON the question sheet so please return all materials. Total 153 points but I will mark out of 150. Individual values follow each question.

1. Here are some true/false questions. The rule is I subtract the wrongs from the rights (but I won't give you negative value for the question as a whole). Each question is worth 3 points and all of the true/false questions are worth 69 points.

   (a) A JFET can be used as both a variable resistor and constant current source/drain.

   (b) The "double diode" model of a bipolar junction transistor can't explain transistor action but it can be used to describe the small signal behaviour.

   (c) There are situations where we treat a -15 V supply like it is at ground.

   (d) The desired input/output characteristics when building a current amplifier are the same as when building a voltage amplifier.

   (e) The value of the forward gain A is always important when designing an amplifier.

   (f) There are many types of motion sensor and they are all transducers.

   (g) With a bit of work an instrinsic semiconductor could be used as a temperature sensor.

   (h) Output resistance (R_o' or r_o) isn't really that important when trying to maintain a consistent voltage gain for a load connected to a simple BJT amplifier. All you need to do is turn up the collector supply voltage.

   (i) Positive feedback comes about when AB is negative.

   (j) Schmitt triggers use a comparator at some stage.

   (k) You have an inverting amplifer based on an operational amplifier and you remove the feedback resistor. The output goes to one of the rails.

   (l) You can assume that V_{BE} is constant when analysing the series feedback common-emitter amplifer.

   (m) RS latches by themselves really have no purpose; they are just components of more complicated and useful flip-flops.

   (n) There isn't really any use for amplifiers that can't work at 0 Hz.

   (o) When a circuit reaches a "3 dB" point the output voltage has dropped to $3^{-1} = 1/3$ of its maximum value.

   (p) You know what components to use to build a fixed voltage DC power supply using electrical power from a building outlet.

   (q) It takes fewer complementary MOSFETs to build a NAND gate than an AND gate.

   (r) Semiconductors are really very similar to metals like aluminum and copper but when you add the donor and acceptor impurities the conductivity is lowered to make them "semi" conductors.

   (s) An amplifier is "passive" when you don't have any potentiometers to adjust.

   (t) You have the oscilloscope in dual channel mode and are looking at the input and output of a circuit as a function of the frequency. You notice that the output is dropping but the phase is not changing. This is what you expected. True or false?

(u) Not only are log scales really convenient for plotting large ranges of frequency and gain/attenuation but there are really important bits of information on them you might not get from a linear scale.

(v) You can use the ideal diode approximation with turn-on voltage to describe rectifier ciruits.

(w) (And just because I like to have fun with true and false or 1's and 0's respectively.) The answers to the 3 previous questions represent R, S, and Q_n. Give Q_{n+1} as "True" or "False".

2. There was also a request for multiple choice. Please give the correct answer to each question for 4 points. For each wrong answer I will subtract 2 point (but I won't give you negative for the question)

   (a) Complete the following statement. A potentiometer is

      i. an actuator that the converts voltage to a position.
      ii. a sensor that converts angular position to a resistance.
      iii. used to measure voltage i.e. a potential "meter".
      iv. None of the above correctly completes the given statement.

   (b) An amplifier has an ideal voltage gain of $A_V = -13$. It has an input resistance of 10 kΩ and an output resistance of 0.080 kΩ. The source has a voltage of 0.5 V peak-to-peak and a resistance of 0.5 kΩ. You measure the output with an oscilloscope. Which of the following statements is true:

      i. You are making measurements with an oscilloscope so you find that the V_o/V_i gain is 22.3 dB.
      ii. The oscilloscope will load the output so the gain will be signicantly less than 22.3 dB.
      iii. Yes, the gain is likely 22.3 dB but this will be frequency dependent for any real amplifier.
      iv. You can't give the gain in dB since it is an inverting amp.

   (c) A high-pass filter is constructed of a $C = 4.7$ μF and $R = 10$ kΩ. The 3dB point is

      i. 3.4 Hz
      ii. 3.4 kHz
      iii. 3.4 V
      iv. $3.4j$ Hz where $j = \sqrt{-1}$

   (d) A diode is meant to allow current to pass in one direction but not in the other. How does this work?

      i. The diode itself is triangle-shaped like the circuit symbol so it is very difficult for electrons to go backward (like a lobster trap).
      ii. The reason above is not quite correct. It is the depletion region that is triangle shaped.
      iii. It is a $p - n$ junction and applying a bias has a different effect on the diffusion and drift currents.
      iv. The reason above is not quite correct. It depends on transistor action and you use an undoped part of the diode to act as a base.

(e) Which of the following statements about bipolar junction transistors is *false*

i. The hybrid model can be used to determine the values at the Q-point.

ii. They come in pnp and npn versions.

iii. They have a stray capacitance that is important at high frequencies.

iv. The small signal output can be modelled as a current source in parallel with a fairly large resistor when looking at small signal behaviour.

(f) Correctly complete the following statement: Field effect transistors

i. rely on magnetic field for their operation which comes from a layer of iron on the gate.

ii. operate identically to bipolar junction transistors except that electric fields are larger.

iii. are extremely flexible and can be used as voltage controlled resistors, current drains, and voltage-controlled digital switches

iv. draw large input currents so require a safety resistor on the gate.

(g) Correctly complete the following statement: Sequential logic circuits are distinct from combinational logic circuits because:

i. feedback is used so that the current state of the output is used in determining the next or sequential state of the ouptut.

ii. it isn't possible to determine the output of a sequential logic circuit. There is always a random element so they are used for random number generators.

iii. combinational circuits are based on NAND and NOR gates and you use IF...THEN gates for sequential logic.

iv. All of the above statements correctly complete the given statement.

3. Draw the circuit described in Question 2c. Make a sketch of the input and the output signal that you would see on the oscilloscope at the 3 dB point. What use could you imagine for this circuit? (8)

4. Draw the circuit described in Question 2b with a 0.22 kΩ load. Give voltage across and current through the load. Give the current gain and the true power gain. (8)

5. (a) Reproduce the schematic shown in Figure 1 in your exam paper and label as appropriate for an n-channel JFET. (3)

(b) Suppose that V_{DS} and V_{GS} are set appropriately so that the JFET is acting as a constant current drain for some load connected to the drain. Make a sketch of the shape of the depletion region (can add it to your previous sketch if you like). (3)

(c) Make a sketch of I_{DSS} versus V_{GS} for a typical JFET. (3)

(d) I have never asked you to do this before but suppose that you replace the n-channel JFET with a germanium npn BJT. Add its curve to the sketch you just made with the correct signs and scales for what is now V_{BE}. (3)

6. Consider the transistor amplifier circuit shown in Fig. 6. The h_{FE} of the transistor is 95. It is a germanium-based transistor.

(a) Stating your assumptions calculate the DC or quiescent current through the base, the collector, and V_o. Based on your experience with transistors is this a good operating point? Why or why not? (7)

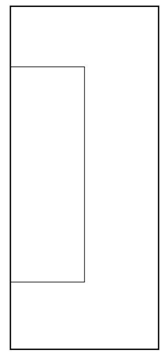

Figure 1: JFET schematic for Question 5

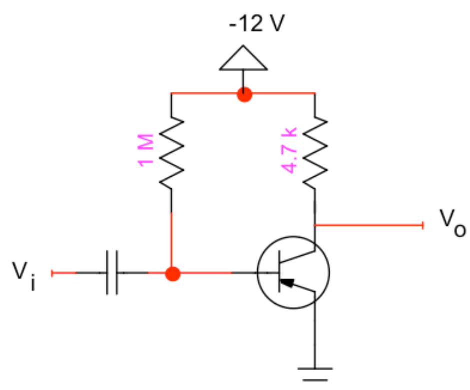

Figure 2: Single-transistor amplifier for Question 6.

(b) Use the diode model of the base-emitter junction to give you an estimate of h_{ie} and g_m. (Don't need to state the model; just use the formulas.) (3)

(c) You don't need to construct the small signal model but use the formula to give the small-signal voltage gain. If you are stuck on previous questions just give a reasonable g_m (with units) and do the calculation. (4)

(d) You should find a large amount of gain for this circuit but the input resistance is pretty low and is equal to h_{ie}. How big of a coupling capacitor is needed on the input if you want the low frequency cutoff to be 50 Hz? (Assume that the source resistance is small.) (2)

(e) What are two of the disadvantages of this circuit compared to the later ones we built using negative feedback? (4)

7. Two of the assumptions used when analysing op-amp ciruits are that the two inputs are at the same voltage and that no currents are drawn by the inputs. How do these assumptions mesh with the "ideal op-amp" assumptions? (As a first step state the ideal voltage op-amp assumptions.) Pick your favourite op-amp circuit and derive the expression for the voltage gain. (8)

$$V_{\text{amplitude}} = \sqrt{2}\, V_{RMS} \tag{1}$$

$$A_V = \frac{V_{out}}{V_{in}} \tag{2}$$

$$A_V(\text{ideal}) = \frac{V_{out,\text{OC}}}{V_{in}} \tag{3}$$

$$V = IR \tag{4}$$

$$R_{Th} = R_N = \frac{V_{\text{OC}}}{I_{\text{SC}}} \tag{5}$$

$$\text{Gain (dB)} = 10 \log_{10} \frac{P_2}{P_1} \stackrel{*}{=} 20 \log_{10} \left| \frac{V_2}{V_1} \right| \tag{6}$$

$$Z_R = R \tag{7}$$

$$Z_C = (j\omega C)^{-1} \tag{8}$$

$$Z_L = j\omega L \tag{9}$$

$$\text{Gain (closed-loop)} = \frac{A}{1 + AB} \tag{10}$$

$$f_{3\text{dB}} = (2\pi RC)^{-1} = (2\pi\tau)^{-1} \tag{11}$$

$$\text{Gain (non-inverting)} = \frac{R_1 + R_2}{R_2} \;, (R_1 \text{ connected to the output}) \tag{12}$$

$$\text{Gain (inverting)} = -\frac{R_1}{R_2} \;, (R_1 \text{ connected to the output}) \tag{13}$$

$$V_{out}(t) = -\frac{1}{RC} \int_0^t dt'\, V_{in}(t') + \text{constant} \tag{14}$$

$$V_{out} = -RC\, \frac{dV_{in}(t)}{dt} \tag{15}$$

$$V_{out} = -(V_1 + V_2)\frac{R_1}{R_2} \;, (R_1 \text{ connected to the output}) \tag{16}$$

$$V_{out} = (V_1 - V_2)\frac{R_1}{R_2} \;, (R_1 \text{ connected to output and ground}) \tag{17}$$

$$\text{(Gain)(Bandwidth)} \sim \text{(unity gain bandwidth)} \tag{18}$$

$$\frac{S}{N}\text{ratio} = 20 \log_{10} \left(\frac{V_S}{V_N} \right) \tag{19}$$

$$\vec{J} = \sigma \vec{E} \tag{20}$$

$$\sigma = e(n\mu_e + p\mu_h) \tag{21}$$

$$np = 4 \left(\frac{k_B T}{2\pi\hbar^2} \right)^3 (m_e m_h)^{3/2} \exp\left(-\frac{E_g}{k_B T} \right) \tag{22}$$

$$n_i = p_i \tag{23}$$

$$I(V) = I_S \exp\left(\frac{eV}{k_B T} \right) - I_S = I_S \left\{ \exp\left(\frac{eV}{k_B T} \right) - 1 \right\} \approx I_S \exp(40\, V) \tag{24}$$

$$I_C = h_{FE} I_B \tag{25}$$

$$I_C \approx -I_E \tag{26}$$

$$h_{fe} \approx h_{FE} \tag{27}$$

$$g_m \equiv \frac{1}{r_e} = \frac{dI_C}{dV_{BE}} \approx 40|I_C| \tag{28}$$

$$h_{ie} \approx \frac{1}{40|I_B|} = \frac{h_{fe}}{g_m} \tag{29}$$

$$dI_C = \left(\frac{\partial I_C}{\partial I_B}\right)_{V_{CE}} dI_B + \left(\frac{\partial I_C}{\partial V_{CE}}\right)_{I_B} dV_{CE} = h_{fe}\, dI_B + h_{oe}\, dV_{CE} \tag{30}$$

$$dV_{BE} = \left(\frac{\partial V_{BE}}{\partial I_B}\right)_{V_{CE}} dI_B + \left(\frac{\partial V_{BE}}{\partial V_{CE}}\right)_{I_B} dV_{CE} = h_{ie}\, dI_B + h_{re}\, dV_{CE} \tag{31}$$

$$A_V \approx -\frac{R_C}{R_E + r_e} = -\frac{g_m R_C}{g_m R_E + 1} \text{ (feedback config)} \tag{32}$$

$$A_V \approx -\frac{R_C}{r_e} \text{ (common emitter or decoup. cap.)} \tag{33}$$

$$r_i = R_1 // R_2 // r_b \tag{34}$$

$$r_b = h_{ie} + (h_{fe} + 1) R_E \text{ (common emitter)} \tag{35}$$

$$r_o = R_C \left(\frac{1 + h_{oe} R_E}{1 + h_{oe}(R_E + R_C)}\right) \tag{36}$$

$$f_c = \{2\pi C_{in}(R_{\text{source}} + r_i)\}^{-1} \text{ (coupling capacitor)} \tag{37}$$

$$f_{co} = \{2\pi C_E (R_E // r_e)\}^{-1} \text{ (decoupling capacitor)} \tag{38}$$

$$f_\beta = \{2\pi (C_{b'e} + C_{b'c}) r_{b'e}\}^{-1} \text{ (high-f hybrid-}\pi\text{)} \tag{39}$$

$$f_\beta \approx \frac{40 I_E}{2\pi h_{fe(0)} C_{b'e}} \tag{40}$$

$$f_T \approx \frac{40 I_E}{2\pi C_{b'e}} \tag{41}$$

$$\frac{V_o}{V_i} = \left\{1 - \frac{5}{(\omega CR)^2} - j\left(\frac{6}{\omega CR} - \frac{1}{(\omega CR)^3}\right)\right\}^{-1} \tag{42}$$

$$f = \frac{1}{2\pi CR\sqrt{6}} \text{ (phase-shift oscillator)} \tag{43}$$

$$A_V = -\frac{1}{29} \text{ (feedback } B \text{ of phase-shift oscillator)} \tag{44}$$

$$\frac{V_o}{V_i} = \left\{3 - j\left(\frac{1 - \omega^2 R^2 C^2}{\omega CR}\right)\right\}^{-1} \text{ (Wein-bridge oscillator)} \tag{45}$$

$$I_{DSS} = I_{DSS0}\left(1 - \frac{V_{GS}}{V_P}\right)^2 \tag{46}$$